Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **VCC**
2. **G=N. A**
3. **A**
4. **H=N. B**
5. **B**
6. **I=N. C**
7. **C**
8. **VSS**
9. **D**
10. **J=N. D**
11. **E**
12. **K=N. E**
13. **NC**
14. **F**
15. **L=N. F**
16. **NC**

**.052”**

**.064”**

**14**

**12**

**11**

**3 2 1 15**

**7 8 9 10**

**4**

**5**

**6**

**CD40**

**49UB**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref: CD4049UB**

**APPROVED BY: DK DIE SIZE .052” X .064” DATE: 5/31/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .011” P/N: CD4049UBH**

**DG 10.1.2**

#### Rev B, 7/19/02